Abstract

of attestation master's degree work subject:
" Investigation of the hardware implementation of embedded systems for image processing and sound " by
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Actuality of work

Analysis image processing is an integral part of digital signal processing. This direction is very important in science. And now, many studies aimed at optimizing existing and developing new methods of compression, encoding, storing both images and video.

This thesis project is devoted to reviewing ways to implement, as well as applying the algorithm JPEG2000, which is designed to compress the image and is based on the discrete wavelet transform (DWT). Work considered by the work of the algorithm for CPU, CUDA and Xilinx Spartan-3A.

The object of research is the JPEG2000 algorithm on different platforms (CPU and GPU), as well as the implementation of the algorithm of one-dimensional DWP Le Gall (5, 3) on the FPGA to evaluate the performance and cost of implementation, which are the subject of research.

The purpose of work

The purpose of work - evaluation of JPEG2000 image compression algorithm and sold fiberboard blocks for different platforms for its further use in scientific, military and industrial.

Tasks solved in work

1. Study of the structure of the algorithm JPEG2000 and work the main blocks. The implementation of this algorithm based on the CPU and CUDA.
2. Realization of one-dimensional three-level fiberboard Le Gall (5,3) on

FPGA Xilinx Spartan-3A.

3. Compare the realizations of the parameters of cost and performance. Construct tables and graphs. Make conclusions about the advantages and disadvantages of applying the DWT module.

The achieved results

Solving the tasks put in-process, an author protects:

• results of the structure of the algorithm JPEG2000 and work the main blocks. The implementation of this algorithm based on the CPU and CUDA;

• experimentally investigated and proved the effectiveness of the proposed hardware of the algorithm of ID DWT Le GAL (5,3);

• experimentally investigated and proved the effectiveness of the algorithm of JPEG2000 for image proccesing on CUDA GPU;

Scientific novelty

Scientific novelty of the work is to conduct a comparative analysis, in which it was shown that the use of technology CUDA, greatly accelerates the calculations in comparison with the standard implementation at CPU, although inferior to the hardware implementation on FPGA. Also consider the hardware implementation of the algorithm based on a one-dimensional DWT lifting scheme. Direct implementation of the DWT (in the form of filters, which use convolution) inferior to the implementation of lifting scheme because it uses more resources and operations and, accordingly, are most critical path that is not conducive to optimizing the clock time.

Practical value

Practical value of work consists in the following:

• experimentally investigated and proved the effectiveness of the proposed hardware of the algorithm of ID DWT Le GAL (5,3);

• experimentally investigated and proved the effectiveness of the algorithm of JPEG2000 for image proccesing .

Conclusions

1. Study of the structure of the algorithm JPEG2000 and work the main blocks. The implementation of this algorithm based on the CPU and CUDA.

2. Comparative analysis, in which it was shown that the use of technology CUDA, greatly accelerates the calculations in comparison with the standard implementation at CPU, although inferior to the hardware implementation on FPGA. Also consider the hardware implementation of the algorithm based on a one- dimensional DWT lifting scheme. Direct implementation of the DWT (in the form of filters, which use convolution) inferior to the implementation of lifting scheme because it uses more resources and operations and, accordingly, are most critical path that is not conducive to optimizing the clock time.

3. Experimentally, compare the realizations of the parameters of cost and performance of the DWB block.

4. Was made gipotesis for parralel realization of 2D DWT block.

The work contains 86 pages, 41 images, 13 sources.

Keywords: DIGITAL SIGNAL PROCESSING, IMAGE PROCESSING, FPGA, CUDA, IMPLEMENTATION OF THE ALGORITHM, JPEG2000, EVALUATION VALUE, RTL, VERILOG, JPEG, DWT.